1. A packaged integrated circuit comprising:

a processor;

a volatile memory; and

a cross-point memory.

2. The circuit of claim 1 including a first die and a second die, wherein said processor is on said first die and said cross-point memory is on said second die.

3. The circuit of claim 2 wherein said first die includes a processor and a bus that couples said processor to the volatile memory and the cross-point memory.

4. The circuit of claim 1 also including a phase-change memory.

5. The circuit of claim 1 including a package containing stacked dice.

6. The circuit of claim 1 wherein said package is a folded stacked package.

7. The circuit of claim 2 wherein said first die includes a processor and a non-volatile memory.

8. The circuit of claim 1 including a non-volatile memory.

9. The circuit of claim 1 including a ball grid array package.

10. A method comprising:

providing a processor and a cross-point memory on separate dice; and

packaging said cross-point memory and said processor in the same package.

11. The method of claim 10 including packaging a volatile memory on a separate die in said package.

12. The method of claim 10 including packaging said processor and said cross-point memory in a folded stacked package.

13. The method of claim 10 including packaging a phase-change memory in said package.

14. The method of claim 10 including providing a bus on said die with said processor and coupling said processor to said cross-point memory through said bus.

15. The method of claim 10 including stacking said dice on top of one another.

16. The method of claim 10 including packaging a volatile memory in the same package with said processor and said cross-point memory.

17. The method of claim 10 including providing a ball grid array on said package.

18. A packaged integrated circuit comprising:
a first die including a processor; and
a second die including a cross-point memory.

19. The circuit of claim 18 including a third die with a volatile memory.

20. The circuit of claim 18 including a bus on said first die coupling said processor to said cross-point memory.

21. The circuit of claim 18 including a phase-change memory.

22. The circuit of claim 18 including a plurality of stacked dice.

23. The circuit of claim 18 including a folded stacked package.

24. The circuit of claim 18 including a ball grid array package.